ABSTRACT

A capacitive element C_1 having a small leakage current is formed by utilizing a gate oxide film 9B thicker than that of a MISFET of a logic section incorporated in a CMOS gate array, without increasing the number of steps of manufacturing the CMOS gate array. The capacitive element C_1 has a gate electrode 10E. A part of the gate electrode 10E is made of a polycrystalline silicon film. The polycrystalline silicon film is doped with n-type impurities, so that the capacitive element may reliably operate even at a low power supply voltage.